FOR IMMEDIATE RELEASE

Enhancing IT system energy efficiency by optimizing LSI supply voltage for tolerable error rate of processing applications

Error tolerance of 1% reduces energy consumption by 7%

Tokyo, Japan, June 10, 2014 --- Hitachi, Ltd. (TSE: 6501, “Hitachi”) today announced the development of technology to enhance the energy efficiency of IT systems by optimizing the supply voltage of incorporated LSIs in accordance with the error rate tolerable in computational results for a given application (tolerable error rate). Conventional IT systems have been designed so that, regardless of installed applications, the error rates are set at almost zero. Through simulations, Hitachi discovered that by just tolerating image noise at a level unnoticeable by humans (a tolerable error rate of 5%), it is possible to reduce the energy consumption of the entire system by 19%. Further, for a tolerable error rate of 1% which would increase practical applications, energy consumption is reduced by 7%. The technology developed will serve as an effective concept to reduce energy consumption in future IT systems when device scaling of LSIs advance further and device variations become physically unavoidable.

The evolution of IT equipment has been driven by lower energy consumption, lower costs and higher performance as a result of advances in LSI device scaling and greater integration. As device scaling progresses and device dimensions approach a nanometer-order near the size of an atom, it is expected that the performance of transistors inside LSIs will become unstable, making it difficult to compensate for bit errors. This will pose a major obstacle to further LSI scaling. Bit errors can be prevented by applying a set high voltage to the LSI, but this raises the problem that the supply voltage to the IT equipment cannot be lowered in order to reduce energy consumption. This problem has surfaced as a serious challenge to reducing the energy requirements of future IT systems.

To address this issue, Hitachi departed from the former design approach for conventional IT systems that focuses on performance, energy consumption and size (LSI integration level), to develop a new design method for a completely new IT system by incorporating tolerable error rate, that is, the stringency of computer calculated output, to the parameters. Characteristics of the newly developed technology are as follows.

- more -

(1) Proposal of a design guideline accounting for tolerable error rate
While energy consumption can be reduced by lowering operating voltage, at the same time, the probability of destroying data (error rate) increases; thus, in order to secure a given error rate, voltage cannot be lowered. If the error rate that current LSIs guarantee (e.g. approx. 10^{-7} for a 1Mbyte SRAM***1**) can be relaxed however, then it will be possible to lower supply voltage. Also, there are many systems where the service value of applications can be maintained despite minimal application errors. Thus, Hitachi proposed a new design approach enhancing energy efficiency in IT systems by incorporating tolerable error rate of an application as a parameter to optimize LSI supply voltage.

(2) Development of a processing method to control LSI supply voltage in accordance with application tolerable error rates
In order to reduce LSI supply voltage without causing IT system failure, it is necessary to maintain the supply voltage for system control-related processing. Hitachi developed a processing method***2** that maintains the supply voltage for system-control-related processing but reduces the supply voltage for other processing in accordance with tolerable error rates. As a result, enhanced energy efficiency was achieved without causing IT system failure.

When simulations were conducted based on the technology developed, in the case of image processing, it was found that 96% of all processing could be conducted with a lower supply voltage, and when an error rate of 5% unperceivable to humans was tolerated, that energy consumption could be reduced by 19%. It was also found that for a tolerable error rate of 1% and 0.1%, that energy consumption would be reduced by 7% and 1%, respectively.

The technology developed proposes a new design method for IT systems incorporating tolerable error rates of applications as a new parameter. While some applications demand an error rate to be as near to zero as possible, there are many other applications that in practicality tolerate a value of 0.1% or 1%. In an era where the issue of rising characteristic variations of LSIs due to device scaling is becoming a reality, this technology enables a significant decrease in energy consumption of IT systems.

A part of the results of this development was presented at the IEEE International Symposium on Circuits and Systems (ISCAS 2014) which was held from 1st -5th June

2014 in Melbourne, Australia.

Notes

*1 SRAM: static random access memory

*2 LSI hardware specifications and LSI-controlling software specifications

About Hitachi, Ltd.

Hitachi, Ltd. (TSE: 6501), headquartered in Tokyo, Japan, delivers innovations that answer society's challenges with our talented team and proven experience in global markets. The company's consolidated revenues for fiscal 2013 (ended March 31, 2014) totaled 9,616 billion yen ($93.4 billion). Hitachi is focusing more than ever on the Social Innovation Business, which includes infrastructure systems, information & telecommunication systems, power systems, construction machinery, high functional materials & components, automotive systems, healthcare and others. For more information on Hitachi, please visit the company's website at http://www.hitachi.com .

# # #

Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.
