14th February 2003

Successful operation of world's smallest 0.3 square millimeter contactless IC chip

- New electrode design facilitating mass production -

Hitachi, Ltd. (NYSE:HIT) has developed a prototype for the smallest IC chip in the world (0.3 sq. mm), and successfully confirmed its operation. The prototype IC chip developed is a contactless type which receives power from electrical waves and wirelessly transmits a 128bit chip-specific number. This chip maintains the same performance levels as the *μ-chip* (pronounced "mu-chip"), the present contactless IC with which Hitachi is currently developing business, while achieving a decrease in size. Further, chip production efficiency was dramatically increased by employing a design where the electrodes are deployed on the upper and underside of the IC chip. This technology will contribute to improvements in mass production of the next generation *μ-chip*.

The *μ-chip* is a minute contactless IC chip that can be buried in paper. Electrical waves are received via an antenna attached to the chip, providing energy, and a 128bit chip-specific number is wirelessly transmitted. As the data is written in ROM (Read-Only-Memory) during the production process, it is impossible to rewrite the data thus guaranteeing high authenticity. By taking advantage of these features, i.e. minute size, high authenticity, contactless, and combining it with Internet technology, a wide range of applications in finance, sales, distribution, transportation, production management, office, sports, entertainment, etc. can be envisioned.

When a chip becomes as small as the *μ-chip*, the connection between the IC chip and the antenna becomes an issue. In previous IC chips, two connecting electrodes were deployed on the chip surface, and connected to the antenna. As the chip becomes smaller, however, so does the electrode itself as well as the space between the electrodes, making efficient connection difficult.

With the 0.3 sq. mm IC chip developed, an antenna structure whereby the electrodes are deployed on the upper surface and underside of the chip, and then the chip is sandwiched by the antenna, was employed. Merits of this structure are that as there is one antenna connecting terminal on each side, the chip surface area is not important; further, even if the chip is upside-down, it will not affect operation. Thus it is possible to assemble the IC chip without taking into consideration whether the chip is facing the right direction, and there is no need for high precision positioning. Further, as it is possible to assemble several chips at the same time, improved production capability is expected. This technology is expected to lead to decreasing *μ-chip* size and improved mass production.

This technology was announced at the International Solid-State Circuits Conference (ISSCC),

which was held from 9th February 2003, in San Francisco, California, U.S.A.

*　　*　　*

Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.

# # #

Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.