"Three-Layer Stacked HJ931 Series" System in Package (SiP) with SuperH™ Microprocessor

— HJ931201BP incorporating microprocessor, flash memory, and synchronous DRAM in a single package reduces mounting area by approximately 65% —

Tokyo, December 4, 2002— Hitachi, Ltd. (TSE: 6501) today announced the development of the "Three-layer stacked HJ931 Series" a "System in Package" (SiP) product incorporating a high-performance Hitachi SuperH™ microprocessor[1] and multiple memory chips in a single package by using three-layer stack structure. Engineering sample shipments are scheduled to begin shipping in December 2002 in Japan. Samples of the first product in the new series, the HJ931201BP, will also commence shipping in December 2002 in Japan. The HJ931201BP incorporates the SH7705, which is built on the SH-3 CPU core designed for use in low-power devices, a 64 -Mbit synchronous DRAM (SDRAM), and a 16-Mbit flash memory.

The series is intended for use in portable devices such as digital cameras and PDAs. In addition to combining a microprocessor and multiple memory chips, such as SDRAM or flash memory, in a single package, something that is normally difficult to accomplish by "System on Chip" (SoC), it employs a three-layer stacked SiP to dramatically reduce the mounting area required. The HJ931201BP, for example, combines three chips—the SH7705, 64 -Mbit SDRAM, and 16-Mbit flash memory—in a 13 mm × 13 mm package that is 1.7 mm (maximum) thick. This results in a reduction of approximately 65% in the mounting area, compared with a configuration using three packages.

< Background >

In recent years there has been increasing demand for more functionality and greater compactness in the market for digital consumer products, in particular portable devices such as digital video cameras, digital still cameras, and PDAs. This has increased the need for SoC products, in which a microprocessor or ASIC is combined with memory on a single chip, and SiP products. Demand for SiP products in particular is growing rapidly due to the advantages they offer over SoC products. These advantages include shorter development times, lower development costs, and ease of application to a wide variety of product requirements and rapidly changing market conditions.

Hitachi already has some SiP (the term multi-chip module or MCM is also used) products in volume production. Examples include side-by-side SiP and two-layer stacked SiP products incorporating a SuperH microprocessor and SDRAM or flash memory or memory and a custom ASIC. The new "Three-layer stacked HJ931 Series" achieves a smaller size by stacking its component chips in three-layers.

- more -

< About this product >

The features of the "Three-layer stacked HJ931 Series" are described below.

(1) Achieves a smaller size

The HJ931 Series combines in a single package the SH-3 CPU core product of SuperH, a high-performance microprocessor with a proven track record in consumer products, and multiple memory chips. Its three-layer stacked structure greatly reduces the mounting area required, compared with the use of multiple packages, and makes it possible to develop more compact systems overall. (The HJ931201BP reduces the mounting area by approximately 65%, compared with a configuration using three packages.) In addition, having the microprocessor and memory in a single package means that the user does not need to design a bus to link the individual chips. The simplifies the design of the system and shortens the product development time.

(2) Reduced Electro-magnetic Interference (EMI)

Greater compactness means shorter circuit board wiring, which in turn reduces susceptibility to electromagnetic noise and allows more stable high-speed operation.

(3) Short development time for SiP products

SiP product development takes only about five to six weeks from the point at which the specifications are decided to the point when samples are ready. (Note that this is in cases where existing LSI chips are employed.) It will be also possible to incorporate custom ASIC chips.

The microprocessor used in the HJ931201BP is the SH7705, which is built on the SH-3 CPU core designed for use in low-power devices. It has a fast operating frequency of 133 MHz and a low internal logic operating voltage of 1.5 V. This makes it ideal for portable products such as PDAs that require high performance and low power consumption.
(http://global.hitachi.com/New/cnews/E/2002/0722/index.html)

The package uses the LFBGA 240-pin configuration and contains a total of three chips: the SH7705, 64-Mbit SDRAM, and 16-Mbit flash memory. It uses a three-layer stacked structure to achieve a size of 13 mm × 13 mm and a thickness of 1.7 mm (maximum).

Hitachi plans to expand its series of "Three-layer stacked SiP" to include products with more than three chips as well as products containing custom ASIC chips. There are also plans for future upgrades to microprocessors with faster operating frequencies, etc.

< Development Tools >

The E10A card emulator is also available as a support tool for designing systems incorporating the "Three-layer stacked HJ931 Series".
Notes: 1.   SuperH™ is a trademark of Hitachi, Ltd.

< Typical Applications >

- Mobile devices such as digital video cameras, digital still cameras, and PDAs
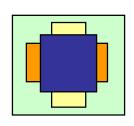- Compact digital consumer electronic products

< Price in Japan >(For Reference)

Product Code	Installed Microprocessor	Installed Memory	Package	Sample Price (Yen)
HJ931201BP	SH7705 (133 MHz)	64-Mbit SDRAM 16-Mbit flash memory	LFBGA 240-pin 13 mm × 13 mm × 1.7 mm (max.)	5,000

< Specifications >

Product code	HJ931201BP
MPU	SH7705 (SH-3 core)
Memory	64-Mbit SDRAM × 1, 16-Mbit flash memory × 1
MPU Operating frequency	Internal bus: 133 MHz
	External bus: 66 MHz
Operating power supply voltage	External (VDDQ): 3.3 V
Operating temperature	0°C to +70°C
External dimensions	LFBGA 240-pin, 0.65 mm pin-pitch
	13 mm × 13 mm × 1.7 mm (max.)
Features	• Microprocessor and multiple memory chips in a single package • 3-layer stacked structure for compact package • Ideal for low-power consumption systems

< Structure of "Three-layer stacked SiP" >(Reference)

• HJ931201BP

1. Top View

Top layer: CPU
Middle layer: Flash memory
Bottom layer: SDRAM

2. Cross Section

3-Stage Stacked Structure