Hitachi Announces Development in SDRAM Embedded Circuit Technology, Reducing Operating Power by 40%

- 49% Reduction in Access Time also Achieved in the 0.28 sq. mm Circuit Area -

TOKYO, Japan, August 6, 2001 Hitachi, Ltd. (NYSE:HIT) today announced that it has developed new circuit technology, "SDRAM Mode Control Scheme", which is able to reduce both operating power and access time in SDRAMs, used in standard memories. This technology, incorporated in a circuit area of only 0.28 square millimeters, was found to reduce at a maximum, power consumption by 40% and access time by 49%, in SDRAMs. Further, as the same effect can be obtained by incorporating this embedded circuit, it is expected to find application in various CPU and MPU circuits as IP (Intellectual Property).

Broadly, mobile devices are composed of the CPU, the memory (DRAM) and the display device. Among these, power consumption by the DRAM accounts for 10-20% of total power consumption and therefore, reducing DRAM power has been a technical issue. Further, compared to the CPU, as the access time of the DRAM is slow, and limits the performance of the mobile device, reducing the access time of DRAM was another requirement. In the past, DRAM power consumption could be reduced through improvements in semiconductor process technology, enabling the DRAM operating voltage to be lowered. However, continuation of this method is thought to be to a detriment to access time and data retention characteristics.

Thus a new memory control scheme, "SDRAM Mode Control Scheme", was developed to achieve lower power consumption and faster access time in SDRAMs. The read operation of the SDRAM consists of three procedures: (1) transfer of the data from memory cells to the sense amplifiers, (2) output of the data from the sense amplifiers, and (3) clearing the data in the sense amplifiers. Since approximately half the operating power of the SDRAM is dissipated in operation (1), the target was to reduce this power consumption. If the data in sense amplifier is not cleared but maintained, i.e. to work the sense amplifiers as a cache memory, and the data which the CPU requests remains in the sense amplifiers, then it is possible to reduce the operating power by eliminating the operation (1). The newly developed "SDRAM Mode Control Scheme" is an excellent scheme to substantially reduce SDRAM operating power by determining whether the sense amplifiers should be worked as a cache memory or not.

The mechanism for determining whether to operate the sense amplifiers as a cache memory or not, i.e. to clear or not clear, is shown below:

(1) If the requested data from the CPU is in the sense amplifier, which is working as a cache memory, i.e. a “hit”, it predicts that the next access will also result in a “hit”, and the data in the sense amplifier is maintained.

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(2) If the requested data from the CPU is not in the sense amplifier, which is working as a cache memory, i.e. a “miss”, it predicts that the next access will also result in a “miss”, and the data is cleared not to work the sense amplifier as a cache memory.

As a result, it was possible to minimize the operations of data transfer from the memory cell to the sense amplifier and the data clear in the sense amplifiers, and therefore achieve both a reduction in SDRAM power consumption as well as access time.

The developed scheme was evaluated using several benchmark programs, and it was found that the operating power consumption and access time were reduced by 40% and 49%, respectively, compared to a conventional SDRAM control. Further, it is possible to design this scheme with an area of 0.28 sq. mm and it can be easily added to the CPU as an embedded IP circuit block.

The developed scheme will be presented at the International Symposium on Low Power Electronics and Design (ISLPED '01) to be held on August 6 - 7, 2001 in Huntington Beach, California, USA.

<Explanation of Terms>

(1) SDRAM (Synchronous DRAM): A high-speed DRAM that has a synchronous operation with a clock signal. At present, SDRAM is the standard DRAM.
(2) Sense Amplifier Circuit: A circuit which amplifies, and maintains data from the memory cell in DRAMs.

Hitachi, Ltd., headquartered in Tokyo, Japan, is one of the world's leading global electronics companies, with fiscal 2000 (ended March 31, 2001) consolidated sales of 8,417 billion yen ($67.9 billion*). The company manufactures and markets a wide range of products, including computers, semiconductors, consumer products and power and industrial equipment. For more information on Hitachi, Ltd., please visit Hitachi’s Web site at http://global.hitachi.com

* At an exchange rate of 124 yen to the dollar.

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