FOR IMMEDIATE RELEASE

Development of CMOS LSI technology for 100Gbit Ethernet optical transceivers

75% Reduction in Power Consumption Compared to Conventional Gearbox LSI

Tokyo, February 22, 2011 – Hitachi, Ltd. (NYSE: HIT / TSE: 6501, "Hitachi") today announced the successful prototyping of a low-power CMOS[*1] gearbox LSI conforming with international standards[*2], which was developed for optical transceivers as part of the effort to reduce power consumption in routers and network equipment to be used in the 100 gigabit (Gbit) Ethernet[*3] (henceforth, 100GbE). Optical receivers convert optical signals and electrical signals. The 100GbE CMOS gearbox[*4] LSI functions to convert the transmission rate and number of channels, converting the 4 channel × 25 gigabit per second (henceforth, Gb/s) electrical signals received from the network into 10 channels × 10Gb/s electrical signals which can be used within the equipment, and vice versa. Until now, a high-speed gearbox LSI based on SiGe[*5] process technology was used for this purpose, however, the achievement of a low-cost and low-power LSI based on the CMOS process was desired. The prototype 100 GbE gearbox LSI fabricated employs the four-phase clock circuit scheme[*6] using CMOS process technology, and achieves operation with a low power consumption of 2W, which is approximately one-quarter that of a SiGe gearbox LSI.

This work was partially supported by the "Universal Link"[*7] project of the National Institute of Information and Communications Technology (NICT), Japan.

Network traffic continues to dramatically increase each year with the rapid development of the broadband environment and the increasing use of high-definition video contents in this age of broadcast and communication convergence. As a result, the need exists for a communication network that provides both high speed and large capacity. In current internet communication, the Ethernet with a communication speed of 10Gb/s is widely used, however, to enable even higher speed, technology for a next generation 100GbE (10 times faster than the current level) was internationally standardized in June 2010. Today, technology development to conform with this standard is being conducted worldwide however a major issue of how to reduce the increasing power consumption which grows proportionally with increasing speed, remained.

- more -

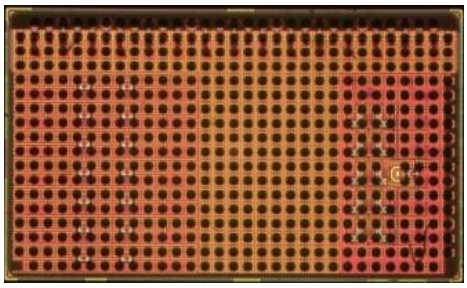
Against this backdrop, Hitachi developed a prototype low-power CMOS gearbox LSI for optical transceivers used in routers and network equipment conforming with the 100GbE international standards. The technology developed includes the "four-phase clock circuit" which maintains the data processing speed of the LSI while reducing the circuit operating speed by 75%, and implementing this in the 25Gb/s interface circuit of the CMOS gearbox LSI. In addition, the CMOS interface (SerDes)[*8] circuit developed in 2010 by Hitachi which has a low power consumption characteristic of 0.98mW per 1Gb/s, was employed in the prototype CMOS gearbox LSI.

Verification tests confirmed that the developed CMOS gearbox LSI operated with a power consumption of 2W; namely, a quarter that of a conventional SiGe gearbox LSI. The CMOS gearbox LSI developed can be applied to not only the 100GbE applications but also in signal transmission between LSIs in information-processing equipment such as servers and routers, and is expected to widely contribute to low power consumption of information-processing equipment.
These results will be presented at the International Solid-State Circuits Conference (ISSCC 2011), to be held from 20th to 24th February 2011 in San Francisco, U.S.

Details of circuit scheme developed

A four-phase-clock circuit scheme to realize lowpower consumption

In the receiving circuit of the 25Gb/s interface circuit, a circuit scheme that determines the level and phase of the received data by using four (phase) clocks with phase differences of 90 degrees, was applied. Through this approach, the interface is operated at a clock rate of 6.25GHz (a quarter of the bit rate) while maintaining the data-processing speed of the LSI, and power consumption is also reduced.
In addition, in a conventional receiving circuit, a receiving clock signal is generated by, first, distributing a high-speed 12.5GHz clock from a common PLL[*9] to four channels in the 25Gb/s interface circuit and then uses a phase-control circuit; a process consuming a large amount of power. A four-phase clock reducing this power consumption was achieved by placing a PLL in each channel of the receiving circuit, dispensing with the need for a power-hungry phase-control circuit. Further power conservation was achieved through this new circuit scheme by controlling the clock frequency allocated to each channel to a low-speed of 625MHz.



Prototype low-power CMOS gearbox LSI (3.7 mm × 6.3 mm)

Note *1: CMOS: Complementary Metal-oxide Semiconductorr

*2: IEEE 3802.3ba (June 2010).

*3: 100 gigabit Ethernet: A standard global Ethernet transmission system to achieve transmission speeds of 100 Gb/s using optical fibers.

*4: Gearbox LSI: An LSI which converts the transmission speed and number of channels for 100Gb data signals to 10:4 or 4:10 (e.g. 10-channels × 10Gb/s to 4-channels × 25Gb/s, and vice versa).

*5: Silicon germanium: A semiconductor material in which silicon is doped with a trace of germanium.

*6: Four-phase clock circuit scheme: A scheme which employs four clocks so that each clock has a phase difference of 90 degrees with reference to a reference clock; namely, each clock has a time delay of a quarter with reference to each other.

*7: Universal link: Basic electrical-signal-processing technology, developed between 2008 and 2010, which freely transmit multiple 100Gb-class signals within or between LAN within an range of 1000km.

*8: SerDes: Acronym for SERializer/DESerializer. A transmission method which converts multi-bit digital signals in series or in parallel, and transmits it as one digital signal. It is widely used in optical and electrical transmission of data volume above 1 gigabit.

*9: PLL: Acronym for phase-locked loop. A circuit that matches the frequency and phase of an input reference clock with those of the output clock. By placing a frequency de-multiplexer in a PLL circuit loop, it is possible to make the output-clock frequency oscillate in synchronization with input-clock frequency.

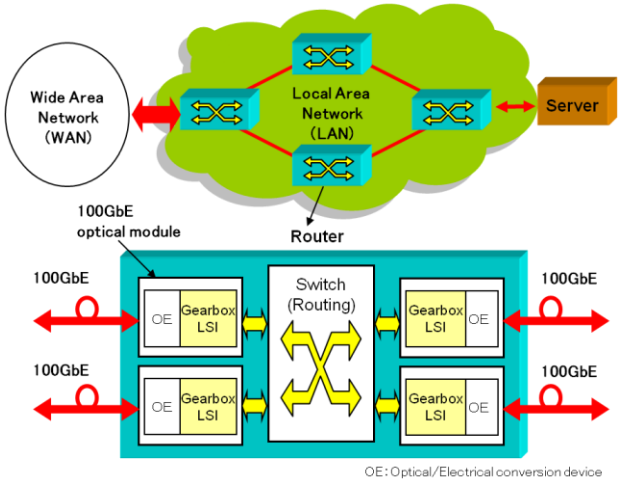


Figure 1. 100GbE LAN and gearbox LSI

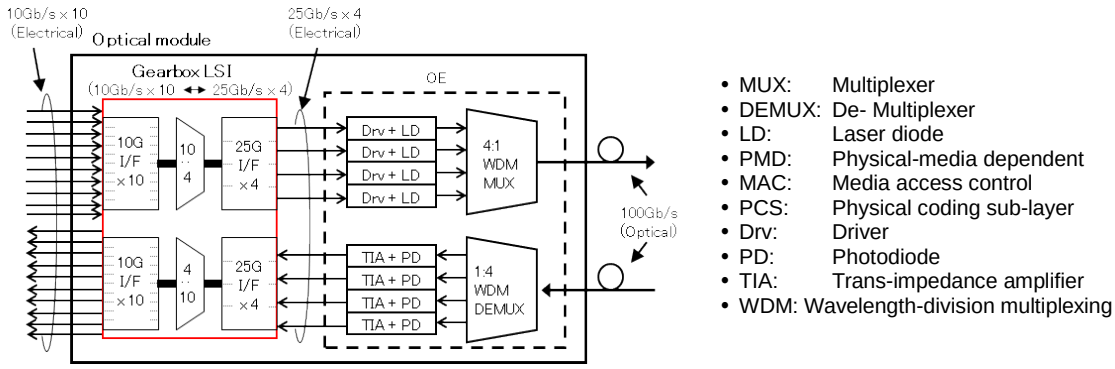


Figure 2. 100GbE Optical module

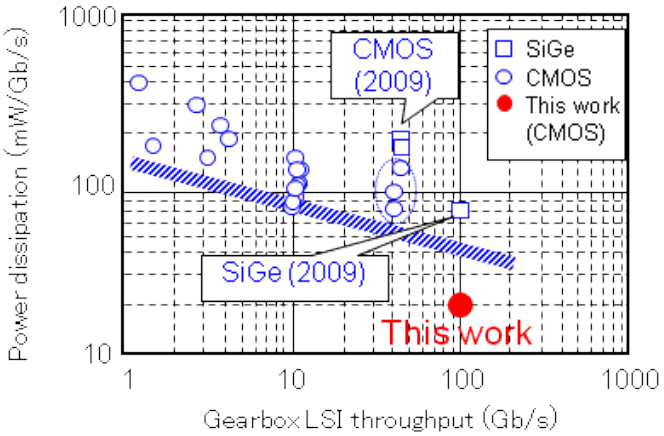


Figure 3. Technical benchmark

About Hitachi, Ltd.

Hitachi, Ltd., (NYSE: HIT / TSE: 6501), headquartered in Tokyo, Japan, is a leading global electronics company with approximately 360,000 employees worldwide. Fiscal 2009 (ended March 31, 2010) consolidated revenues totaled 8,968 billion yen ($96.4 billion). Hitachi will focus more than ever on the Social Innovation Business, which includes information and telecommunication systems, power systems, environmental, industrial and transportation systems, and social and urban systems, as well as the sophisticated materials and key devices that support them. For more information on Hitachi, please visit the company's website at http://www.hitachi.com.

# # #

Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.
