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Hitachi develops transceiver circuit technology for servers to handle large capacity and high-speed transfer (total transfer rate of 168 Gb/s) with low power consumption

---Low-noise design for 20 percent less power consumption than an existing product---

Tokyo, June 27, 2008 --- Hitachi, Ltd. (NYSE: HIT / TSE: 6501) today announced the development of transceiver circuit technology with a 21-lane transceiver, each lane having a transfer rate of 8 Gigabit/second (Gb/s), for a total transfer rate of 168 Gb/s. As well as increasing the performance in transfer within server equipment, which has become a bottleneck when large amounts of data must be transferred at high-speeds, the technology realizes substantial power savings when applied to server, storage and communications devices. Hitachi has already adopted a transceiver with a transfer rate of 5 Gb/s in an LSI circuit for information–communications devices and placed this product on the market. The new technology can reduce power consumption by 20 percent compared with that LSI circuit, which is now in actual service*1. The current aim for the new technology is entry into practical service within one or two years by solving problems such as the increase in power consumption that will accompany the larger capacities and higher speeds at the 8-Gb/s target transfer rate of the next generation.

*1: Realization of 20 percent lower power consumption is relative to Hitachi's LSI circuit for information–communications devices that is currently in practical service.

The demand for larger data capacities and higher transfer rates in computer-network communications has grown in recent years. Performance in transfer within the server equipment that supports data communications has become a bottleneck in data processing on networks. Data transferred in server equipment goes through a printed circuit board within the body of the server equipment that has slots and connectors and is called a 'backplane'. Multiple circuit boards are connected to the backplane, and signals are transmitted between separate boards via the backplane. The signal transmission distance is 20 to 80 cm. As the distance increases, so does the distortion in waveforms of the data signals transmitted on the backplane, until this prevents the sending of correct signals. Manufacturers of information and communications devices are trying to solve this problem by developing signal processing technology to correct signal distortion.

Various methods involving signal-processing technology are being considered. Waveform equalization, including technology for predicting the distortion of the signal waveform and sending signals to compensate for the predicted distortion, and technology to accentuate received signals which have been weakened by distortion, is effective and widely employed. Furthermore, as superior waveform equalization for high-speed data transfer at rates above 5 Gb/s, decision feedback equalization (DFE) and other signal-processing techniques are said to be coming into service. However, such technology has certain disadvantages, including logic circuits that are larger and consume more power due to their complex design. Furthermore, new logic circuits for error correction are required because once an error occurs in DFE, it is propagated to subsequent data in the sequence.

Hitachi has now increased the transfer rate on the backplane to 8 Gb/s without using complicated signal-processing technology such as DFE. Also, with low-noise design technology, the company has succeeded in equipping a test chip with the 21-lane transceiver, each lane providing an 8-Gb/s transfer rate. Adopting this circuit in LSI circuits for information–communications devices will contribute to better performance in transfer within devices and to reduced power consumption.

Features of the newly developed technology for transceiver circuits are as follows.

(1) Low-noise design

Designs of the clock generator and clock recovery circuit are optimized to suppress variation in clock-signal timing. Furthermore, technology to substantially suppress power-supply ripple generated in circuit operation and to reduce variation in circuit-delay time due to power-supply ripple has been adopted. These optimized designs reduce the amount of noise in signals, enabling high-speed transfer over long intervals without requiring complex signal-processing technology such as DFE.

(2) Power-saving design

Avoiding complex signal-processing technology such as DFE and the accompanying logic circuits for error correction reduces both the size of logic circuits and power consumption. A power-saving design with only 160 mW/lane means that low-power LSI circuits are possible, even when multiple lanes are mounted. The delays in data transfer produced by DFE and the associated logic circuits for error correction are also avoided.

(3) High reliability and flexibility

The low-noise and power-saving design means that even the dense mounting of multiple

lanes does not cause transfer performance to suffer, and reduces bit error rate on the backplane to less than 1/1000 of that for currently available technology. As the technology makes mounting multiple lanes possible, it facilitates the efficient transmission of parallel data for data processing by computers. Furthermore, as specific signal processing is not employed, the technology can meet various needs according to the specifications and architecture employed in devices.

The technology has been developed according to the Harmonious Green Plan*2, Hitachi's technology and product development plan that promotes greater power savings in major IT products. The company also made a presentation on the technical details of the development at the 2008 Symposium on VLSI Circuits, an international conference on semiconductor integrated circuits held in Honolulu, USA, from June 18, 2008.

*2: This is a plan to promote all kinds of technological development to reduce the power consumption of major IT products and provide power-saving products. Through product development in accord with the plan, the company plans to cut down a cumulative total of roughly 330,000 t of CO_2 over the five years from 2008.

About Hitachi, Ltd.

Hitachi, Ltd., (NYSE: HIT / TSE: 6501), headquartered in Tokyo, Japan, is a leading global electronics company with approximately 390,000 employees worldwide. Fiscal 2007 (ended March 31, 2008) consolidated revenues totaled 11,226 billion yen ($112.2 billion). The company offers a wide range of systems, products and services in market sectors including information systems, electronic devices, power and industrial systems, consumer products, materials, logistics and financial services. For more information on Hitachi, please visit the company's website at http://www.hitachi.com.

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