Hitachi and the University of Tokyo develop
Low-Power Consumption LSI Technology
for Future Energy-Efficient Supercomputers
Program pattern based control of operating frequency and
substrate voltage for power conservation

Tokyo, June 20, 2008 --- Hitachi, Ltd. (NYSE: HIT / TSE: 6501) and Professor SAKURAI Takayasu of the Institute of Industrial Science of the University of Tokyo announced that by finely controlling the processors used in supercomputers, they have co-developed technology which enables the power conservation in LSIs consisting of integrated processors. This research was conducted as part of work funded by the Ministry of Education, Culture, Sports, Science and Technology-Japan (MEXT).

The technology developed makes use of the ability to identify which processor is performing a calculation by program pattern during a large-scale computation on a supercomputer. By incorporating a circuit (resistor circuit) to control the processor operating frequency and substrate voltage, it makes possible to lower the operating frequency of non-performing processors. Further by controlling the substrate voltage, leakage current can also be reduced; thus making it possible to save power in the LSIs as well as the supercomputer as a whole. A prototype LSI with four processors was fabricated with a 90nm process for experimental purposes. Verification tests with this prototype chip yielded a maximum possible reduction of 50% in power consumption.

In the face of growing demand for energy-efficient environment-conscious electronic information equipment, higher processing speed in addition to decreasing power consumption has been a major issue in supercomputers. This development achieves both high performance and low power consumption, and

provides basic technology towards achieving an environment-conscious large-scale supercomputer for scientific calculations.

Supercomputers are used in a wide range of applications from providing information services, such as weather forecast information, which support our daily life to pharmaceutical drug development based on the collection of cutting-edge technology. Supercomputer development has been advancing at a rapid pace with processing power increasing by approximately one thousand times over ten years. Although the supercomputer executes its large-scale numerical computation through massive parallel processing, this high performance is highly dependent on the performance of the core processors. To date, advances in LSI performance including processors, has been driven by device miniaturization, however power consumption has also increased in conjunction with this miniaturization, and in the near future, with further increase in performance, power consumption of supercomputer is predicted to reach the 10 MW-level.

Two major factors play a role in this increase in LSI power consumption; operating power and leakage current which flows when the LSI is idle in a stand-by state, i.e. not in operation. Until now, advancement in operating pattern analysis in system LSIs used in compact information devices such as mobile phones has enabled the development of methods to reduce leakage current in idle LSIs by controlling the substrate voltage. Depending on the application program, idle processors also exist in supercomputers. It was believed that finely controlling the operating frequency and substrate voltage of those processors to reduce operating power and leakage current, might contribute to decreasing the overall power consumption of the supercomputer.

In response to this challenge, the joint research team of Hitachi and Professor Sakurai of the University of Tokyo worked on the development of circuit technology to finely control operating frequency and the substrate voltage for a system where an extremely large number of processors operate in parallel, such as in supercomputers.

Results of this development are as follows:
(1) Analysis of processor operation (in supercomputers) during the execution of large-scale scientific numerical computations

In general, in parallel computing there are processors that only perform parallel computation, and processors that communicate with other processor and prepare for computation as well as perform computations. It is known that these two kinds of processors operate at different times and undertake different computational loads, e.g. while the latter is preparing for computation, the former which only conduct computations are in an idle state. As processing time is required to change the operation frequency and substrate voltage of processors, the research team analyzed the operating status of processors during the execution of large-scale numerical computations. As a result of detailed analysis, it was found that the difference in operation timing could be used to change the substrate voltage, and further, that this change could be even more finely controlled by a program.

(2) Circuits design to control LSI for low power operation according to program pattern

A technique where resistor circuits, which set the substrate voltage and operation frequency of LSIs, are installed to reduce the operation frequency of idle processors, as well as reduce leakage current by raising the threshold voltage through controlling the substrate voltage, was proposed. When parallel computation is executed, the processors which prepare for computation direct the contents of the task to be executed to the processors which only conduct calculations. When this occurs, the operating frequency is lowered and substrate voltage is raised in the processors which were not allocated a task in order to suppress leakage current during this idle state. When the idle processor is again allocated a task, the preparation time before calculation commences is used to change the operating frequency and substrate voltage, thus enabling execution without degrading performance.

Using a 90nm process, a prototype LSI with four processors was fabricated for experimental purposes and basic operation was confirmed. Application of the new techniques developed, yielded a maximum reduction of 50% in LSI power consumption depending on the large-scale scientific computation. This result is expected to become basic technology in the realization of an environment-conscious supercomputer which achieves both high performance and low power consumption.

These results will be presented at the 2008 Symposium on VLSI Circuits, to be held from June 18 - 20, 2008, in Honolulu, Hawaii, U.S.A.

■**About Hitachi, Ltd.**

Hitachi, Ltd., (NYSE: HIT / TSE: 6501), headquartered in Tokyo, Japan, is a leading global electronics company with approximately 390,000 employees worldwide. Fiscal 2007 (ended March 31, 2008) consolidated revenues totaled 11,226 billion yen ($112.3 billion). The company offers a wide range of systems, products and services in market sectors including information systems, electronic devices, power and industrial systems, consumer products, materials, logistics and financial services. For more information on Hitachi, please visit the company's website at http://www.hitachi.com.

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