FOR IMMEDIATE RELEASE

Operation verified on world's smallest 0.05 mm x 0.05 mm "contactless powder IC chip"
One-ninth the size of previous prototype, enabling insertion in paper

Tokyo, 13th February 2007 --- Hitachi, Ltd. (NYSE:HIT / TSE: 6501) announced today that it has developed and verified operation of a 0.05 mm × 0.05 mm (millimeter), 5μm (micrometer) thick contactless RFID IC chip (henceforth 0.05mm chip), the smallest and thinnest in-the-world, to date. The 0.05mm chip is a smaller version of the 0.4 × 0.4 mm^2 "μ-Chip"(*1) currently being marketed by Hitachi, maintaining the same level of functionality. The 0.05mm chip was achieved by employing 90nm SOI(*2) technology and memory technology using electron beam lithography. The surface area of the 0.05 mm chip is one-ninth the size of the 0.15 × 0.15 mm^2, 7.5μm thick contactless IC chip(*3) (henceforth 0.15mm chip) announced by Hitachi in February 2006. The range of applications for contactless IC chips will be further expanded by this drastic decrease in chip size, such as its use in authentication of gift vouchers and stock certificates, and will open the way to new markets for RFID tags.(*4)

The "μ-Chip" is one of the world's smallest contactless IC chips which uses an external antenna to receive radio waves (2.45 GHz microwaves), and transforms it to energy to wirelessly transmit a 128 bit (10^{38}) unique ID number. As the data is written during the fabrication process using ROM (Read-Only-Memory), it is impossible to rewrite the data and thus provides a high level of authenticity. By combining its other features such as compactness, high authenticity and contactless communication, with Internet technology, the "μ-Chip may" be utilized in a broad range of applications such as security, transportation, amusement, traceability and logistics.

Hitachi has been working on technology such as increasing communication distance and decreasing antenna size, whilst maintaining those merits, to enable a broader range of applications for the "μ-Chip". The enhanced thinness of the chip developed and its compactness will further broaden the range of possible applications, including its use in securities like gift certificates and a large variety of certificates. Further, as with the 0.3mm IC chip, the new chip has a double-surface electrode, and therefore despite its even smaller size, connection with the external antenna can be easily achieved, and high productivity maintained.

Features of the IC chip developed

(1) ID data stored in compact ROM
ROM memory which can provide a 1 bit memory cell in 1 transistor was used to compactly store the ID data (128 bits) in a small surface area. Each bit of the ID data is "recorded" in the memory cell during the chip fabrication stage by the presence or lack of

wiring, thus dispensing with the need for write circuitry and enabling a smaller chip. Further, as the data is determined by the presence or lack of wiring, the “memory” is highly reliable, and thus will perform stably even under environmental conditions (e.g. temperature, noise) which may be considered relatively harsh for IC chips. Furthermore, it is open to application of advances in LSI scaling technology.

(2) ID data written in ROM with electron beam lithography equipment
As the ID data is “recorded” by the presence or lack of wiring, electron beam lithography is used. As the ID data is different for each RFID chip, it is not practical to prepare a new mask each time to render the wiring pattern representing the ID data on to a silicon wafer, as is the conventional process. Electron beam lithography was therefore employed to directly render the individual wiring pattern of each chip on to the silicon wafer, dispensing with the need for a mask. In general, the slow throughput of this method is an issue. To overcome this, a new processing method was developed. As each RFID chip is 0.05mm × 0.05 mm and ultra-small, a batch of 10,000 chips was classified as 1 group. Each group was then treated as a 5mm × 5mm chip, and processed at one time. Thus compared to processing each 0.05mm chip individually, processing speed was increased approximately 50 times.

The significant decrease in size of the chip developed represents a dramatic increase in the number of chips which could be produced from a single silicon wafer, and translates to a simple expected productivity increase of nine-fold compared to the 0.15mm chip, and 60-fold compared to the current product “µ-Chip” (0.4mm × 0.4mm).

These results will be presented at the IEEE International Solid-State Circuits Conference (ISSCC 2007), held from 11th - 15th February 2007, in San Francisco, California, U.S.A.

Notes

*1 “µ-Chip” and the “µ-Chip” logo are trademarks or registered trademark of Hitachi, Ltd., in Japan and other countries.

*2 Silicon-on-Insulator (SOI): In the SOI process, an insulation layer and a monocrystalline silicon layer (referred to as the SOI substrate) are first formed upon the base silicon substrate. The transistor is then formed on this SOI substrate. As this structure allows the transistors to be kept separate despite decreasing the distance between the devices, it is an effective method for decreasing overall chip size.

*3 The 0.15 x 0.15 mm, 7.5 µm thick, double-surface electrode IC chip presented at ISSCC 2006. It is different from the IC chip currently in mass production.

*4 Radio frequency identification (RFID): An automatic and wireless device using radiowaves for recognition and authentication.

About Hitachi, Ltd.
Hitachi, Ltd., (NYSE: HIT / TSE: 6501), headquartered in Tokyo, Japan, is a leading global electronics company with approximately 356,000 employees worldwide. Fiscal 2005 (ended March 31, 2006) consolidated sales totaled 9,464 billion yen ($80.9 billion). The company offers a wide range of systems, products and services in market sectors including information systems, electronic devices, power and industrial systems, consumer products, materials and financial services. For more information on Hitachi, please visit the company's website at http://www.hitachi.com.

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