❖*This article has been translated from the original release in Japanese for your convenience*❖

A new low power SRAM circuit reducing standby leakage current to $^{1}/_{100th}$
Applied to a new SOI transistor with double gate structure

Tokyo, 1st November 2005 --- Hitachi, Ltd. (NYSE:HIT / TSE: 6501) today announced a proposal for a new memory cell control method which achieves a high performance low power SRAM using transistors with double-gate structure FD-SOI (Fully Depleted-Silicon On Insulator)(*1) excelling in low power performance. The new SRAM controls the electrical potential of the substrate node (back gate) of each column of memory cells in response to a write or read operation. When the performance of the new circuit was verified using simulation, operating margin was improved, write operation speed was increased by 30% and standby leakage current reduced to $^{1}/_{100th}$ that of conventional SRAMs using bulk transistors. This fundamental technology is expected to open the way for the use of high performance SRAM in SoC (system-on-chip) in mobile information terminals, which require low power components.

The SoC, a key device in mobile information terminals, is required not only to have high-speed processing feature but also very low power requirements, to extend the battery life of the information terminal. The SoC employs a large number of SRAM as on-chip memory, and therefore SRAM performance directly influences the performance of the whole SoC. Scaling of SRAM in recent years has resulted in increased leakage current during standby (the period during which the circuit is not operating) and performance variation, making it increasingly difficult however, to achieve both high-speed and low power. In particular, this increase in variation results in a decrease in operating margin, which prevents the stable operation of the memory cell, and has become a major problem in SRAM design. In the 90nm node, many circuit techniques were employed to overcome this problem. Beyond the 65nm node, however, it has been pointed out that circuit techniques alone will be insufficient, and that development of new technology, including device structure, is required.

Given this challenge, Hitachi is proposing a new SRAM cell using FD-SOI transistors based on a double gate structure(*2), and has verified by simulation that leakage current can be reduced and operating speed increased.

The newly developed memory cell control method, controls the electrical potential of the substrate (back) gate of each memory cell column, for each type of memory cell operation (write, read). Features of the technology developed are as below:

1. Improved operating margin

In the SRAM circuit, two different operations, read and write, are performed on the memory cell. The operations are based on different principles, and therefore require different operating margins. By controlling the electrical potential on the back-gate for each memory cell column, for each type of operation, it was possible to increase the operating margin necessary for each type of operation.

2. Decreased leakage current

In the SRAM circuit, even during the standby mode when there is no access to the circuit, it is necessary to apply a voltage to the circuit in order to retain its data. Leakage current, that is current that "leaks" from the transistor, requires greater power and thus is a problem. By controlling the back-gate potential, it became possible to decrease leakage current.

Simulation estimation of the proposed SRAM circuit was conducted using actual measurement results of FD-SOI devices. Compared to conventional SRAM using bulk transistors, leakage current was approximately $^{1}/_{100th}$, and as operating margin was improved, operating speed was increased by 30%.

This fundamental technology is expected to open the way for the use of high performance SRAM in SoC in mobile information terminals, which require low power components.

These results will be presented at the 2005 Asian Solid-State Circuits Conference (A-SSCC 2005), held in Hsinchu, Taiwan, from 1st - 3rd November 2005.

Technical Terms & Notes:

(*1) Fully Depleted Silicon on Insulator (FD-SOI): In a conventional semiconductor IC, the transistor is formed on a silicon substrate. In the case of the SOI, an insulator layer is formed above the silicon substrate, and the transistor is formed on the insulator layer. The transistor is formed in an ideal environment as it is surrounded by insulators. In an FD-SOI transistor, the thickness of the SOI layer is less than 50 nm, and the channel region is fully depleted. Transistor performance is high as the drive (On) current is high and the leakage (Off) current is low.

(*2) A new FD-SOI transistor with smaller process variation and smaller leakage current than conventional SOI transistor was used. Further, control of current characteristics was improved by the use of two gate electrodes, i.e. a double-gate transistor. (In a conventional transistor, the current characteristics are controlled by one gate electrode.)

About Hitachi, Ltd.

Hitachi, Ltd., (NYSE: HIT), headquartered in Tokyo, Japan, is a leading global electronics company with approximately 347,000 employees worldwide. Fiscal 2004 (ended March 31, 2005) consolidated sales totaled 9,027.0 billion yen ($84.4 billion). The company offers a wide range of systems, products and services in market sectors including information systems, electronic devices, power and industrial systems, consumer products, materials and financial services. For more information on Hitachi, please visit the company's website at http://www.hitachi.com

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