New CAM for IPv6 generation Network Routers

- Enabling six times more IP address storage than before -

Tokyo, July 20, 2004 ---Hitachi, Ltd. (NYSE:HIT / TSE:6501) in cooperation with Elpida Memory, Inc., have developed a new compression encoding method for CAM (Content Addressable Memory: memory with search functions, used in network routers), which enables twice the number of IP (Internet Protocol) addresses to be recorded in the same chip area. When this technology is combined with general purpose DRAM memory cell technology, which has excellent integration capabilities, the number of IP addresses may be increased to six times the conventional number. This fundamental CAM technology will contribute to increasing performance and reducing costs of network routers in the IPv6 (Internet Protocol version 6) generation, which will be accompanied by a surge in the number of IP addresses.

Technological development in various areas such as backbone equipment, routers, switches, software, is being conducted to achieve the next-generation network society using IPv6 capable of allocating 10^{38} (128 bit) IP addresses.

In the field of semiconductor devices, CAM has been receiving attention as the device for IPv6 generation networks. This device is used in routers to forward and filter signals, is characterized by its data table memory and high speed search functions.

The CAM memory cell is composed of 2 memory devices, which stores the IP addresses, and a comparator. CAM is considered a suitable device for the IPv6 generation, as the forwarding address of a signal received can be retrieved from a pre-registered list of IP addresses, thus capable of handling the large number of IP addresses. Conventional CAM, however, incorporates a redundancy where it is only able to store three values (of information) in a memory cell which, in principle, can store four values. Further, it employs an SRAM memory cell structure, which carries with it difficulties in increasing of integration and memory capacity, thus limiting its suitability for the IPv6 generation.

To overcome these problems, Hitachi and Elpida proposed a new CAM structure suitable for the IPv6 generation, capable of further integration and memory increase, resolved the redundancy issue to enable increased number of IP addresses to be registered, and confirmed successful circuit operation by simulation. Two features of the new CAM are described simply below:

(1) **A new concept encoding scheme, resolving the redundancy issue in the memory cell.** The new scheme encodes IP addresses represented by a binary data (0, 1), into quaternary data for every 2 bits, and stores every digit into the four memory elements. Thus the new CAM is able to store twice the range of IP addresses in the same area as a conventional CAM.

(2) **IP address match detector circuit technology:** During a search for a pre-registered IP address, a match detector circuit is necessary to determine whether the comparison result shows a match or not. A new detector circuit consisting of two transistors was proposed as the detector judges signals from each memory block storing the quaternary data in four memory elements. CAM can perform search operations with only a minimal increase in area as the number of transistors in the proposed detector is small.

When the amount of memory used was compared for IP addresses stored in a currently operating router, the new encoding method was found to require on average half that of the conventional encoding method. Further, when the technology is combined with general-purpose DRAM-based memory cell technology, with high integration characteristics, it is possible to increase the number of IP addresses recorded by a factor of six, for the same chip area. This technology will be fundamental in achieving high performance, low cost network routers in the IPv6 generation when IP addresses are expected to exponentially increase.

These results were presented at the Symposium on VLSI Circuits, held in Hawaii, U.S.A. from 17th June 2004.

■ **Technical Terms:**

1) **DRAM:** Dynamic Random Access Memory. Data is maintained in the memory by periodic refresh operations. Two values (binary data) is stored in one memory cell using one MOS transistor and one capacitor.
2) **SRAM**: Static Random Access Memory. Data is retained in memory indefinitely (as long as a sufficient power supply voltage is provided), without any need for a periodic refresh operation. Two values (binary data) is stored in one memory cell using six MOS transistors.

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3) By using the proposed compression encoding scheme, every digit of the IP address is represented by four-bit-string, in which one of four bits is the logic value “1”. Thus, when more than two bits are the logic value “1,” one code can represent multiple IP addresses. Since the number of combinations of the bit-string in a code block is 16 (i.e., 2^4 and 4^2),

this is equivalent to storing one of four variations of data, using the same two number of memory elements as in conventional CAM. Thus, the proposed encoding scheme resolves the redundancy issue in the memory cell and improves the compression ratio of the range of IP addresses.

About Hitachi, Ltd.

Hitachi, Ltd., (NYSE:HIT/TSE:6501) headquartered in Tokyo, Japan, is a leading global electronics company, with approximately 326,000 employees worldwide. Fiscal 2003 (ended March 31, 2004) consolidated sales totaled 8,632.4 billion yen ($81.4 billion). The company offers a wide range of systems, products and services in market sectors, including information systems, electronic devices, power and industrial systems, consumer products, materials and financial services. For more information on Hitachi, please visit the company's Web site at http://www.hitachi.com.

About Elpida Memory, Inc.

Elpida Memory, Inc. is a manufacturer of Dynamic Random Access Memory (DRAM) with headquarters based in Tokyo, Japan, and sales and marketing operations located in Japan, North America, Europe and Asia. Elpida offers a broad range of leading-edge DRAM products. Elpida is a joint venture company formed by NEC and Hitachi on December 20, 1999 and has been in operation since April 2000.

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