Development of an On-chip SRAM Circuit featuring the World's Lowest Standby Current of 25 μA/Mbit and 90% Reduction in Leakage Current under Low-speed Operation

Tokyo, February 27, 2004 -- In collaboration with Renesas Technology Corp. and SuperH, Inc., Hitachi, Ltd. has developed new SRAM (static random-access memory) circuit technology for application as the on-chip memory of system LSIs used in mobile phones. The new concepts behind this developed technology are the achievement of the world's lowest standby current of 25 μA/Mbit and the reduction in leakage current to one tenth of the conventional level under low-speed operation. For applications that require high-performance processing and low power consumption at the same time—such as prolonged viewing of digital terrestrial broadcasts on a mobile phone—this circuit technology significantly reduces power consumption of system LSIs.

In regards to system LSIs for handling multimedia processing for functions such as games and videophone on mobile phones, both "maximization of performance" to enable high-speed processing of massive amounts of data and "minimization of power consumption" to prolong battery life are being demanded. Up till now, the performance of system LSIs has been increased through the scaling-down of the elements that compose the LSI circuit. However, as this scaling-down continues, it has become a noticeably growing problem that power consumption has increased because leakage current flows even while the circuit is not operating. To address this problem, a technique called "power switch control"—which shuts off the power to unused circuit components to prevent the leakage current flowing in them—has been the focus of much attention. However, in addition to incorporating a conventional cache[1] memory, the SRAM for use as the on-chip memory of a system LSI (i.e., in-built memory), a so-called on-chip SRAM, incorporates a URAM (UserRAM[2])—which must hold data even during the standby time (i.e., the time when the CPU does not access the memory). This memory configuration means that the power-switch-control technique cannot be applied to an on-chip SRAM. Accordingly, a way of reducing the leakage current

without shutting off the power supply must be developed.

With the above-described circumstances in mind, Hitachi, Ltd., Renesas Technology Corp., and SuperH, Inc. have developed SRAM (static random-access memory) circuit technology based on the new concept of significantly reducing the leakage current of an on-chip SRAM. This new technology features the two circuit techniques summarized below.

Technique (1): Reducing leakage current during standby by means of "source-line-voltage control"

The "source-line-voltage control" technique—for self control of applied voltage in response to operating temperature and memory-cell performance—was developed. It attains stable operation and leakage-current reduction at the same time. Although it has been known that applying a voltage to a source line effectively reduces leakage current, doing so comes at the expense of reduced memory-cell stability. However, in the case of the developed source-line-voltage control, by applying a voltage to the source line of the SRAM circuit—which is usually at 0-V potential—the leakage current during standby can be reduced.

Technique (2): Reducing leakage current during low-speed operation

During low-speed operation, leakage current accounts for a large proportion of overall power consumption. Given that fact, we have developped a new low-leakage operation mode exclusively for low-speed operation. Under the assumption that all non-accessed memory cells are in standby mode, technique (1) mentioned above can then be applied to substantially reduce leakage current.

Incorporating circuit techniques (1) and (2) described above, a prototype 1-Mbit on-chip memory was fabricated in accordance with the 0.13-μm CMOS rule and experimentally tested. The test results are summarized as follows: technique (1) reduces the power consumption during standby state to a world's-lowest value of 25 μA/Mbit;

and technique (2) suppresses the leakage current in low-leakage-operation mode to one tenth of that under high-speed operation. These techniques represent the basic circuit technology that will be the key to power reduction in system LSIs.

This new circuit technology was presented at the 2004 IEEE International Solid-State Circuits Conference (ISSCC) held in San Francisco from February 14-19, 2004.

Footnotes:

(1) Cache memory: a high-speed memory built into the CPU of an LSI chip for improving the overall LSI performance by means of holding frequently used data.

(2) URAM (UserRAM; also known as WorkRAM): a memory for holding often-used data.

Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.
