

## **Development of The World's Highest-Performance Processor Core for System LSIs used in Next-generation Digital Consumer Appliances**

### **—Floating-Point Performance of 2.8G FLOPS and Three-Dimensional Graphics Processing at 36M Polygons/s—**

Tokyo, February 16, 2004 -- Hitachi, Ltd. (TSE:6501, NYSE:HIT), Renesas Technology Corp., and SuperH, Inc. today announced the development of a processor core<sup>\*1</sup>—with the world's highest processing performance of 2.8 GFLOPS<sup>\*2</sup> and 36M Polygons/s<sup>\*3</sup>—for the system LSIs used in next-generation digital consumer appliances. The processor cores are conventionally separated into two independent designs: one for high-speed processing and one for low power consumption; however, in the new processor-core technology, the fundamental parts of the cores are unified. This means that the design period is 30 to 40% shorter than that for the conventional processor core. From now on, it is expected that this processor core will become the core technology for the system LSIs that will underpin the increased functionality expected with the further popularization of digital consumer appliances.

Over the last several years, the dramatic improvements in the functions of digital consumer appliances such as mobile phones, digital cameras, and car-navigation systems have come as a result of the increased performance, decreased power consumption, and reduced cost of the system LSIs at the heart of these devices. In line with the further increases in functionality expected from now on, on top of more improvements in performance and reductions in power consumption and cost, further shortening of the product development time—in response to the shorter product lifecycles expected in the future—is being demanded.

Moreover, in the case of digital consumer appliances, because the required performance and power consumption of system LSIs vary across a broad range of products, a designer has to design LSIs to fit the requirements of these individual

requirements. Up till now, the processor core has been arranged as two systems—one for outstanding calculation performance and the other for extremely low power consumption—and system LSIs have been developed by applying either of these two systems to meet the required LSI specification. However, while meeting the demand for higher performance, it has become necessary to develop processor-core technology that will enable system LSIs for various products to be developed in a shorter time.

In view of the background described above, in collaboration with Renesas Technology and SuperH, Inc., Hitachi Central Research Laboratory has developed a processor-core technology that can provide system LSIs with increased performance—while meeting a wide range of product specifications—in a short development time. Making use of the advantages of the two individually developed systems for a conventional processor core, this new technology integrates the fundamental parts of these systems. The three main features of this technology are summarized in the following.

**(1) Integrated processor core for flexibly meeting a wide range of performance and power specifications**

Since options such as functionality, operating frequency, and applied voltage can be selected from a single master design, this integrated processor core can meet a broader range of performance and power specifications than a conventional two-system processor core and, accordingly, development of system LSIs is easier. Together with its high flexibility in meeting various specifications, the developed processor-core technology significantly shortens the development time for system LSIs.

**(2) High-speed processing through “super pipeline”<sup>\*4</sup> and “super scalar”<sup>\*5</sup> methods**

In addition to the conventional dual-issue super-scalar architecture—used in conventional processor cores for outstanding high-speed processing—the new core technology uses a seven-stage super pipeline architecture to achieve high-speed

processing. In particular, the problem associated with the application of a super pipeline architecture (namely, degradation in performance at a certain frequency) is overcome by means of latency-concealment techniques such as delayed execution<sup>\*6</sup>, early branch architecture<sup>\*7</sup>, and branch prediction.<sup>\*8</sup>

### **(3) Floating-point unit (FPU) with gigahertz-class high performance**

An FPU—which is applied for three-dimensional graphics processing and so on—is configured as a module that can easily give rise to a degradation in that processing performance at a certain frequency. By applying vector-instruction enhancement<sup>\*9</sup> and a high-speed logic-circuit architecture for the first time, the new-processor core technology can provide floating-point performance of an embedded processor equal to that of a high-performance processor with gigahertz operation.

A prototype processor based on the new technologies described above core was fabricated by the 130-nm CMOS process. Under a 1.25-V operating voltage and 250-mW power consumption, this prototype achieved high-speed operation of 400 MHz and performance of 1.8 MIPS/MHz. It also attained a peak floating-point performance of 2.8 GFLOPS and a three-dimensional-graphics basic processing performance of 36M polygons/s—which both represent the world’s highest performance on an embedded processor to date. Moreover, by using these processor-core technologies when designing two LSI systems from one master design, the design time can be reduced by 30 to 40% compared to that when using conventional technologies.

As the core of system LSIs, the newly developed processor-core technology described here is expected to provide more appealing and amenable devices in line with the expected further development of digital consumer products such as car-navigation systems and mobile phones.

This newly developed processor-core technology was presented at ISSCC 2004 (International Solid-State Circuits Conference) held by the IEEE in San Francisco from

February 15 to 19, 2004.

## ■ Terminology

Note \*1: A processor modularized as a part of a system LSI

Note \*2: 28 billion floating-point calculations executed in one second

Note \*3: 3D-graphics basic processing performance of 36 million polygons per second

Note \*4: A method for improving operating frequency by increasing the number of pipeline stages

Note \*5: A method for improving performance at the same frequency by means of executing more than two instructions at once

Note \*6: A latency-concealment method that delays the commencement stages for calculation and data storage

Note \*7: A latency-concealment method that executes the branch instruction at an earlier time than the preceding instruction

Note \*8: A latency-concealment method that predicts branch direction and then executes the branch instruction before direction confirmation

Note \*9: Vector instructions for calculating inner product, matrix-vector product, and square-root reciprocal can be executed four to seven times faster than by the conventional method.

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Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.

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