Development of Power Reduction Techniques for Next-Generation Cellular Phone System LSIs

- Offering lower operating current dissipation for high-performance system LSIs, together with a standby facility allowing quick recovery while keeping standby current low -

Tokyo, February 16, 2004 - Renesas Technology Corp., Hitachi, Ltd. (TSE:6501, NYSE:HIT), and SuperH, Inc. today announced the development of power consumption reduction techniques for high-performance CPU core, and a standby technique enabling quick recovery from the standby state to the active state while keeping standby current low, for use in system LSIs for cellular phones and similar applications.

Trial production using these techniques in system LSI for next-generation cellular phones confirmed the achievement of CPU core performance per unit power of 4500 MIPS/W, and recovery to the active state in the short time of 3 milliseconds (max.) while holding standby current down to 100 μA or less.

As process technology has become finer in recent years, the integration level has improved and logic scale has increased. System LSIs, which implement most system functions in a single chip, have shown a particularly remarkable increase in logic scale, and the greater power consumption associated with higher speed and performance has become a major problem.

Meanwhile, the cellular phone market has seen major expansion in such application areas as games and camera image display, and the third-generation cellular phones seen as future mainstream products are expected to offer even more sophisticated and versatile applications. Higher performance is consequently being demanded of system LSIs for cellular phone use, and performance improvements achieved with faster operating frequencies generally mean higher operating power consumption. Another major concern is how to minimize standby power consumption in order to prolong battery life. One solution adopted is to reduce the standby current by shutting down power to unused modules (function blocks) in the chip. With current technique, however, power must be shut down outside the chip, and all information is lost in the shut-down modules, with the result that recovery from the standby state to the active state takes long time. There has thus been a problem of restrictions on standby state setting.

Against this backdrop, Renesas Technology Corp., Hitachi, Ltd., and SuperH, Inc. have developed techniques that enable operating power consumption to be reduced while increasing the operating frequency and greatly improving the processing capability of a high-performance CPU core, together with a standby technique that allows quick recovery to the active state while minimizing standby current, and have confirmed the effects of these techniques. Details of these techniques are as follows.

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(1) Techniques for reducing the operating current of a superscalar*[1] CPU core

With one kind of CPU core instruction processing architecture, a multi-stage pipeline*[2] is provided and processing is divided into small units which are executed in parallel. To improve performance, the operating frequency can be raised by increasing the number of pipeline stages, but this also results in higher power consumption during operation. Renesas Technology Corp., Hitachi, Ltd., and SuperH, Inc. have now developed a pointer-controlled pipeline technique and an instruction cache memory activation rate reduction technique that prevent increase of operating current dissipation for a CPU core with a 7-stage pipeline.

(a) Pointer-controlled pipeline technique

In conventional pipelining, flip-flop circuits connecting the pipeline stages operate once per cycle, and several times before one instruction is completed, to update data. With this newly developed pointer-controlled pipeline technique, on the other hand, a method has been devised whereby flip-flops operate only once for one instruction. Minimizing the number of flip-flop update operations has resulted in an approximately 25% power reduction compared with conventional pipelining.

(b) Instruction cache memory (IC: instruction cache)*[3] activation rate reduction technique

Increasing the number of pipeline stages generally results in lower branch instruction performance. An effective way of preventing this is to perform instruction look-ahead and prefetch the branch destination instruction. However, instruction look-ahead is a speculative process, and requires an excessive number of instruction cache memory accesses, resulting in increased current dissipation.

This newly developed technique provides fine control of instruction cache activation, as follows.

(1) Instruction cache memory is divided into a number of blocks.

(2) According to states, only the block to be accessed is operated, and other blocks are not.

This control enables the activation rate to be reduced by keeping the operated cache memory area to the essential minimum, and achieves an approximately 45% reduction in cache memory access related current dissipation during system LSI operation.

(2) Standby technique allowing quick recovery while minimizing standby current

A “resume standby mode” has been developed that allowing quick recovery while minimizing the standby current. Details of this technique are as follows.

(a) Circuitry in the chip is divided into a number of areas, each incorporating a power supply switch.

(b) In “resume standby mode”, the power supply is maintained only for SRAM and control registers holding information in the chip. Most chip areas, including the CPU and cache memories, have their power supply shut off by their power supply switches, greatly reducing the standby current.

As the power supply is maintained for circuits holding information for recovery to the operating state, although the standby current is greater than when power to all circuits is cut, it is possible to implement a standby state that allows quick recovery. Also, as this power supply switch control is carried out inside the chip, power supply control from off-chip is no longer necessary.

A test chip employing the above-described techniques was created using a 0.13 μm CMOS process, and the effects of the techniques were evaluated. At a 200 MHz CPU core operating speed (360 MIPS processing performance), power dissipation was 80 mW, and for processing performance per unit power, a world top-level performance power efficiency figure of 4500 MIPS/W was achieved. Maximum current dissipation in resume standby mode was 100 μA or less, and recovery to active state was confirmed to be possible in a short recovery time of 3 milliseconds or less.

These newly developed techniques are effective for use in portable information devices such as cellular phones, and are promising techniques for implementing system LSIs offering high performance together with low power consumption.

These results will be announced at the 2004 IEEE International Solid-State Circuits Conference (ISSCC) being held in San Francisco from February 15.

Notes: 1. Superscalar architecture: A method of increasing computer processing speed by simultaneously executing multiple instructions in one cycle.

2. Pipeline: A CPU successively performs finely subdivided processes such as (1) instruction reading, (2) determination of instruction type, (3) computation, and (4) data storage, and normally the next instruction cannot be started until current instruction processing has been completed. A pipeline enables each subdivided process to be executed independently, making it possible for processing of the next instruction to be started before current instruction processing has finished.

3. Instruction cache: High-speed, small-capacity memory in the CPU, used to store instruction codes that are frequently used during program processing. Fetching instruction codes from the instruction cache enables processing to be speeded up since low-speed external memory need not be accessed.

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Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.
