Hitachi Releases the media processor "BroadGear™ Series" with an improved video processing performance

－An video processing engine was added to the VLIW architecture core, resulting in video processing performance double－

Tokyo,March 31,2003－Hitachi Ltd.,(TSE:6501,NYSE:HIT) today announced the media processor "BroadGear™ Series" (hereafter referred to as the BroadGear processor) whose video processing performance [peak performance 55 GOPS (*1) (at 370 MHz)] is double that of our existing product (MAP-CA). This was a result of adding an video processing engine to the VLIW (*2) and SIMD (*3) architecture CPU core. This product will be released on the 1st of April and sample shipment will also commence.

The BroadGear processor is a processor with high flexibility that can meet diversified media processing standards (*4). The BroadGear highly integrates VLIW CPU core, coprocessors and peripheral interfaces that are necessary to multi-media products into one chip. Because multi-media functions are delivered by application software rather than dedicated hardware, this chip contributes to flexibility, time to market and the reduction in the number of parts. This product is the most suitable for video-centric applications such as video surveillance systems, broadband video distribution, and set-top-boxes.

(*1) GOPS (Giga Operation Per Second): Index to indicate how many calculations can be performed simultaneously per second

(*2) VLIW （Very Long Instruction Word）: Architecture that performs multiple processing in a single cycle by increasing the instruction word length

(*3) SIMD （Single Instruction/Multiple Data）: One of the processing types of the microprocessor to allow the handling of multiple data with a single instruction

(*4) MPEG-2 (Moving Picture Experts Group phase 2), MPEG-4、JPEG2000 (Joint Photographic Experts Group 2000), MP2 (MPEG-1 Audio Layer Ⅱ), NTSC/PAL (National Television Standards Committee/Phase Alternation by Line Color Television), IEC958 (International Electrotechnical Commission 958), etc.

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With the spread of the broadband network, the market of video and image processing centric multi-media products(digital TV, Internet broadcasting, digital video recorders, video on demand (VOD) systems, security and surveillance systems, etc.) has rapidly developed. For those applications, this chip gives high video image performance and flexibility to meet for various standards.

In March 2000, Hitachi (and Equator Technologies, Inc) announced and introduced the media processor "MAP-CA" to meet the high image processing performance and high flexibility specifications required in diversified media processing standards. The "MAP-CA" adopts the architecture based on the VLIW and SIMD, and achieved high image processing performance of 30 GOPS (at 300 MHz).

Because media functions can be programmed in C language, various functions including MPEG encoding/decoding, can be implemented by the application program.

Hitachi is providing a compiler (*5) and an evaluation board (*6) as a tool kit to develop an application program. With this tool kit, media processing can be programmed in C language. This facilitates the development of an application program, thereby remarkably reducing the development period . Hitachi is also supplying typical application software separately. The in-circuit emulator (*7) will be supplied by Sophia Systems Co., Ltd. (Representative Director: Masashi Saito).

(*5) A program to translate a program described in high-level language C into an optimum form

(*6) A board used for operation check and performance evaluation of an application program

(*7) A development tool to analyze error by executing LSI operations on an actual machine

■ Price and shipping time of the new product in Japan (For Reference)

Product name	Sample price	Sample shipment availability
BroadGear	¥10,000/piece	April 1,2003

- The compiler, evaluation board, application software, and in-circuit emulator are options. Information regarding cost and other details can be provided upon request.

■ Home page for product information

http://www.hitachi.co.jp/Div/ddc/english/product/product.html

■ Indication about other companies' trademarks

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■ Outline of Sophia Systems Co., Ltd. <As of March 31, 2003>

- Name: Sophia Systems Co., Ltd. (Company listed in JASDAQ (6942))
- Location of headquarters: Kawasaki-shi, Kanagawa Prefecture
- Foundation: August 1975
- Representative director: Masashi Saito
- Number of employees: 150
- Description of business: Development, manufacturing, sale, repair, maintenance, and consulting information/service operations of electric devices, and staffing service of incidental engineering workers and software workers
- Line of business

Design/automation system

-- Microcomputer development support system (in-circuit emulator), EDA system

Information system, etc.

-- Stock price information system, radio recording/reproducing tool

- For further information on Sophia Systems Co., Ltd., contact:
http://www.sophia.com/

■ References

Person in charge: Kojima
Planning Office, Device Development Center,
Information and Telecommunication Systems
Hitachi, Ltd.
6-16-3, Shinmachi, Ome-shi, Tokyo 198-8512
+81-(0)428-33-2011 (direct dialing)

"BroadGear™ Series", Basic Specifications, and Features

1. Benifits

(1) High performance

-An video processing engine is added to the MAP-CA architecture, resulting in image video processing performance double that. [Peak performance 55 GOPS (at 370 MHz)]

* Performance (at 370 MHz)

16-bit or 8-bit SIMD operation	18GOPS
16-bit or 8-bit AND/OR operation	15GOPS
8-bit SAD (distance operational instruction) operation	37GOPS
32-bit integer operation	2GOPS
Motion estimate operation	55GOPS
Motion compensation operation	16GOPS

(2) Highly integrated functions in one chip

- The BroadGear highly integrates VLIW CPU core, coprocessors and peripheral interfaces that are necessary to multi-media products into one chip.

-Two video outputs can be simultaneously performed.

-Real-time MPEG-4 ASP video encoding is executable in real time.

-Real-time MPEG-2 MP@HL videodecoding.

(3) 0.13 µm CMOS copper metal process

(4) A compiler technologies , that Hitachi has developed for super computers for long time, is adopeted Media processing can be described in C language.

(5) An evaluation board is supplied for debug and performance evaluation of application programs.

(6) Platform solution

Media processing is implemented by software and contributes to:

- High flexibility and expandability

- Add -on applications download services can be, etc.

(7) Lineup

300 MHz and 370 MHz products .

SDRAM and DDR-SDRAM interface .

2. Specifications

Supply voltage (core)	1.3V
Supply voltage (I/O)	3.3/2.5V
CPU	136bit 4-issue VLIW (2-clusters)
Coprocessors	Variable Length Decoder/Encoder Data steamer (DMA transfer engine) Video filter x 2 Motion Estimate/Compensation accelerator Encryption/Decryption module (DES, MULTI2)
Package	597-pin plastic BGA
Process	0.13 µm CMOS process, copper metal

3. Features

● VLIW processor

VLIW architecture that permits simultaneous execution of four instructions

Two-cluster configuration

136bit 4-issue VLIW architecture CPU (2-clusters)

Two 32-bit integer arithmetic units, one 64-bit shuffle/partitioned-add unit, and one 128-bit multi-media arithmetic unit (for each cluster)

Sixty-four 32-bit general-purpose registers (for each cluster)

Four 128-bit local data registers (PLC/PLV) in the multi-media arithmetic unit

Up to 16 MAC operations in one cycle

64 KB 2-way set associative instruction cache

32 KB 4-way set associative 4-port data cache

● SDR/DDR SDRAM controller

64-bit SDR SDRAM/DDR SDRAM interface, supporting up to 512 MB,

supporting up to 8 SDRAM devices

● Variable length Encoder/Decorder

16-bit programmable co-processor with 8KB data memory and 8KB instruction memory

● Data streamer

64-channel DMA controller with 8 KB buffer memory

● Video filter

4 x 5, 3 x 5, or 2 x 5 filter

Processing up to 2015 horizontal pixels

16 KB line buffer memory

Two video filters

- MULTI2 encryption/decryption module (option)
- 56-bit single DES/triple DES encryption/decryption module (option)
- Motion Estimate/Motion Compensation accelerator
- PCI interface

32-bit 33 MHz/66 MHz PCI interface

- Video input interface

Two-channel parallel TCI,

2-channel ITU-R BT.601/656 input, or

1-channel parallel TCI input and 1-channel ITU-R BT.601/656 input

- Video output interface

Two-channel ITU-R BT.601/656 output

One-channel parallel TCI output

Analog RGB output (with a 110 MHz RAMDAC)

One-channel D-Connector output

12-bit/18-bit/24-bit digital RGB output

- Display refresh controller (DRC)

RGB-YCbCr conversion

Hardware cursor

Color palette

- Audio interface

IEC958

I^2S

- Serial interface

UART: 2channel

- Peripheral device control

I^2C

- General-purpose data port (GPDP)

General-purpose 8-bit full duplex data port

- General-purpose input/output port (GIO)

16-bit general-purpose input/output port

- Flash ROM interface

Up to 8 MB supported

- Boundary scan (JTAC)

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Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.
